K_u- AND K-BAND GaAs MMIC VARACTOR-TUNED FET OSCILLATORS USING MEV ION-IMPLANTED BURRIED-LAYER BACK CONTACTS

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Abstract

An all ion-implant, planar process has been used to fabricate high-Q, hyper-abrupt carrier profile, varactor diodes as components of GaAs MMIC VCOs with state-of-the-art performance. These GaAs varactor-tuned FET oscillators operate up to 24 GHz with a tuning bandwidth of 5 GHz in K-band. The high-Q varactors feature a buried N^+ layer created by ion-implantation at up to 6 MEV. Separately masked implanted N^+ areas connect the buried layer to ohmic contacts at the surface. Varactor f_c of 1600 GHz was obtained at 0.09 pF.

INTRODUCTION

Varactor diodes have wide application in microwave circuits, including local oscillators (1)-(7), efficient frequency multipliers (8),(9), and phase-shift elements (10),(11). Potential system applications include receivers, frequency converters, and phased array antennas. However, the use of varactors in GaAs MMICs has been limited by low quality factor (Q). High Q requires a low resistance conduction path from the depletion layer edge to the ohmic contact of the diode. A relatively thick low resistance N^+ back-contact layer under the active layer of the varactor is needed for high Q. Most MMIC processes used to obtain such an N^+ layer are not compatible with the fabrication of FETs, because FETs require semi-insulating material under the active layer. Processes using epitaxial layers are possible, but they require a two-level (at least) mesa etch process that results in a very non-planar surface and a reduction in yield. Previous FET-based VCOs (varactor controlled oscillators) omitted the N^+ back contact, compromising Q. The best reported results (1) for this type of VCO show a maximum Q of 3.3 at 15 GHz; thus, the cut-off frequency, f_c, (product of frequency times Q) is 50 GHz. One way around the problem is to use IMPATT diodes instead of FETs in a VCO (3)-(5), but GaAs IMPATT diodes have excessive high phase noise, which is detrimental to system performance.

A new, monolithic, high-Q, Schottky-barrier varactor process, compatible with FETs, has been developed by COMSAT (12). It uses ion implantations up to 6 MEV to create buried N^+ areas for low-resistance back contacts. This work has drawn heavily on previous studies carried out at NRL (13). Lower energy implants are used to create the other conducting layers required in the MMIC. The process is all ion-implant and planar, and therefore capable of providing high yield. This process has been used by us to fabricate K_u- and K-band FET based VCOs along with discrete FETs and varactors on the same wafer.

VARACTOR DESIGN

The variation of varactor capacity with voltage is often characterized by a parameter, gamma. The capacity, C, is given by the following formula.

$$C = \frac{A}{(V + V_O)^\gamma}$$

Where A and V_O are constants. The varactors were designed to have hyper-abrupt carrier profiles for a γ-value of 1.2. A γ of 2.0 would provide linear variation of frequency with tuning voltage. Instead, the 1.2 value was chosen because computer modeling showed that this reduces the series resistance while providing an acceptable F vs V_t curve. The required carrier profile shape has carrier density vs depth, x, varying as x^α, for $\gamma = 1.2$, $\alpha = -1.167$. With the help of a computer program, this shape was approximated by several silicon implantions modeled as Gaussian distributions (14).

The varactor diode contains the three implanted regions shown in Figure 1. Only the upper portion of the hyper-abrupt profile is implanted in the cylinder below the Schottky barrier. The lower portion is included with the buried layer. This strategy reduces series resistance at low bias values by decreasing the depth at which the current begins to flow parallel to the GaAs surface. Surface contact to the buried layer is provided by multiple low energy N^+ ion implants. Ohmic contacts are formed on this region. The resulting diode structure is planar. Between the GaAs surface and the top of the buried layer, a high resistivity annular ring separates the N^+ and hyper-abrupt regions. It provides electrical isolation and serves as a guard ring for achieving low-leakage high breakdown voltage at the Schottky barrier. The diameter of the Schottky junction is adjusted to provide the various zero-bias capacity values required in the MMIC VCO.

MMIC VCO DESIGN

A common gate FET oscillator circuit topology, Figure 2, was chosen to evaluate the performance of the planar varactor process. This type

of circuit has been shown to be successful for monolithic varactor tuned FET oscillators through K_u-Band (1),(15)-(16). The circuit design was developed using discrete components fabricated by the same process. The chips were characterized and then assembled using short wire-bond interconnects between the GaAs chips, yielding a pseudo-monolithic circuit. This provided sufficient information for the MMIC designs. Several circuit layouts using different combinations of varactors were included to cover different frequency bands. A photograph of one of the MMIC VCO chips is shown in Figure 3. Each design incorporates a 0.5-μm by 150-μm GaAs MESFET, 2 to 4 tuning varactors, thin film capacitors, GaAs resistors, microstrip meander lines, and via-hole grounding.

FABRICATION

The N^+ anode (back contact) region in the buried layer is created by co-implanting Si^+ and S^+ at 6 Mev energy, using a three micron thick plated-gold mask. The same mask was used for the lower energy implants to produce the deep portion of the hyper-abrupt profile. All implantations at energies above 300 keV were performed by Universal Energy Systems, Inc. of Dayton, Ohio. The lower energy implants are masked using AZ 1375J photoresist. These include the upper portion of the hyper-abrupt profile, the FET active layer, and the N^+ connection between the buried layer and the ohmic contact locations. The resulting carrier profile in the GaAs below the Schottky barrier location is shown in Figure 4. The buried layer has measured sheet resistance of 9 to 12 ohms per square. Surface contact to the buried layer is provided by N^+ implants at several energies up to 300 Kev. Ohmic contacts are formed on this N^+ region. The carrier profile of the FET active layer is shown in Figure 5. A single post implant activation step is performed using a silicon nitride cap and rapid thermal anneal at 980°C for 10 s. Process monitoring of the implantation was performed using separate monitor wafers. Carrier profiling and sheet resistance measurements were made on the monitor wafers.

After implant activation, the photo-resist lift-off mask for varactor Schottky contacts and capacitor bottom plates is used to mask a 750 A recess etch. The Ti/Pt/Au metal is then deposited by e-beam evaporation. COMSAT's standard process steps are used for FET gates, air-bridges and electro-plated gold conductors. The 0.5-μm FET gates and portions of the meander lines were defined by e-beam lithography. Other lithographic steps were performed using conventional photolithography.

After front side completion, the wafers are subjected to DC characterization using an array of process monitor patterns and an automatic probing system. Uniformity and reproducibility of 5 percent is obtained. Following these tests, the wafers are thinned to 100 μm, via-holes are etched from the back, and the back side is metalized and electroplated. Dicing is performed face up using a dicing-saw.

MEASUREMENTS

Discrete varactors, fabricated on the same wafer as the MMIC VCOs, were characterized from 2 to 18 GHz to determine the variation of their one-port S-parameters. For this purpose they were mounted in a test fixture at the end of a 50-ohm microstrip line. The varactor cathode was wire bonded to the top conductor of the line. The anode of the varactor and the microstrip line ground plane were both grounded. S-parameter data were fitted to a series RLC equivalent circuit. Excellent fits were obtained. The inductance values were consistent with the wire bond lengths. R and C values found in this way were used to calculate the varactor cutoff frequency, f_c, which determines the quality factor Q for any given frequency. Figure 6 compares the data obtained from the S-parameter measurements at 0, 5, and 10 V across the varactor to the 1-MHz C vs V data for the same diode. The agreement of capacity values is excellent. For a capacity of 0.50 pF, which occurs near zero bias voltage, f_c of this varactor is 100 GHz. This rises to 1600 GHz at -10 V.

Discrete 0.5-μm x 150-μm FETs, fabricated on the same wafer as the MMIC VCOs, were characterized for their 2-port S-parameters from 2 to 18 GHz. A maximum frequency of oscillation of 63.4 GHz was calculated from these data.

The MMIC VCO chips were mounted on Kovar carriers using 0.010-in. thick alumina substrates with tanatalum nitride static protection resistors. DC and RF connections to the MMIC chip are via these substrates. A photograph of the test fixture with a VCO3 die is shown in Figure 7. The gate and drain bias were adjusted separately to optimize tuning bandwidth and RF power output. A small amount of tuning on the RF output line helped to improve the matching of the VCO chip to it.

As shown in Figure 8, tuning bandwidth of over 5 GHz was obtained with up to +5 dBm output power (Figure 9). These data are comparable to those of Rease and Beall (1), but our Q values are higher. This allows a higher maximum frequency to be reached.

CONCLUSION

Commercially available high energy implantation services have been used to develop a planar ion implant process for the fabrication of high-Q monolithically compatible varactors in semi-insulating GaAs wafers. This process was used to fabricate several different MMIC VCOs and discrete varactors. These have exhibited state-of-the-art performance. A tuning bandwidth of over 5 GHz and output power of +5 dBm were obtained from K-band MMIC VCOs. 0.5-pF discrete varactors show a cut-off frequency (product of f times Q) of 100 GHz, which increases to 1600 GHz when the capacity is decreased to 0.09 pF at a bias voltage of -10 V.

High-Q varactors are useful in many microwave applications. We believe that this high-yield process makes it practical to include them in MMICs.

ACKNOWLEDGMENTS

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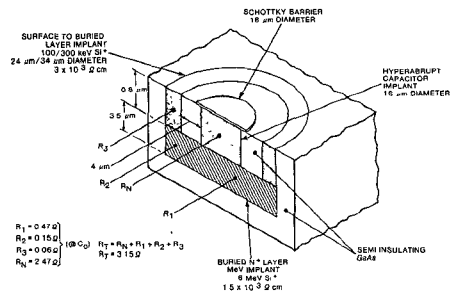

Figure 1. Cross-Section of the Planar Ion-Implanted Hyperabrupt Varactor Diode

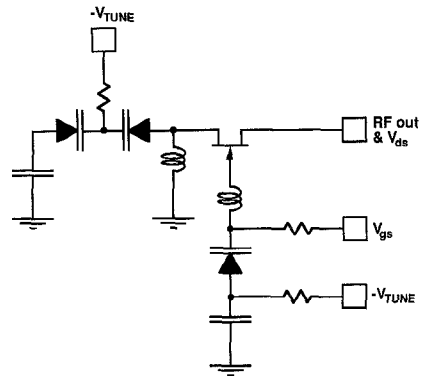

Figure 2. Typical VCO Schematic

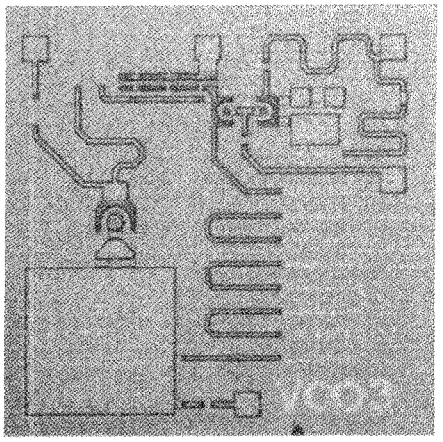

Figure 3. Photograph of a Typical 0.75-μm Square MMIC VCO Chip

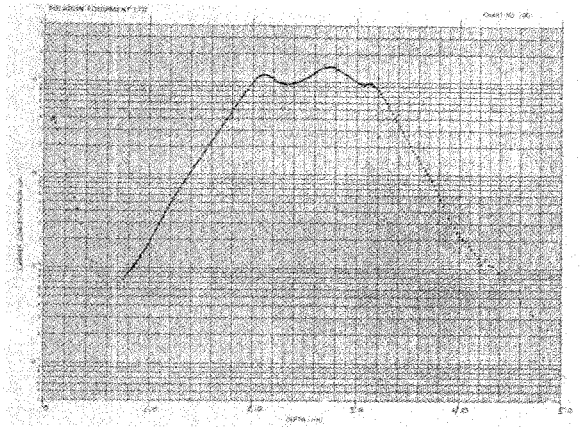

Figure 4. Ion Implanted Carrier Profile for Varactor Diodes Showing Both Shallow and Buried Portions Before the 750 A Recess Etch

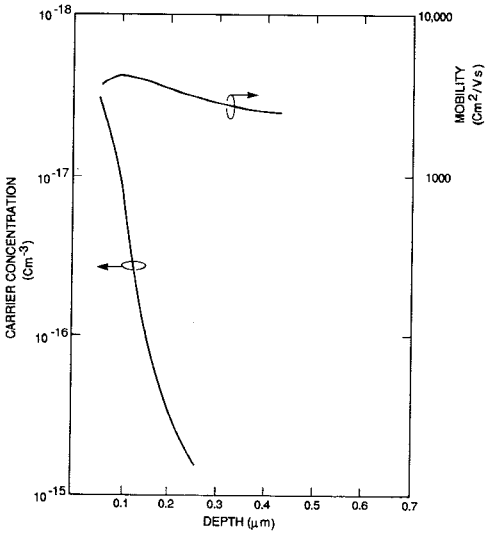

Figure 5. Ion Implanted Carrier Profile for the FET Active Layer

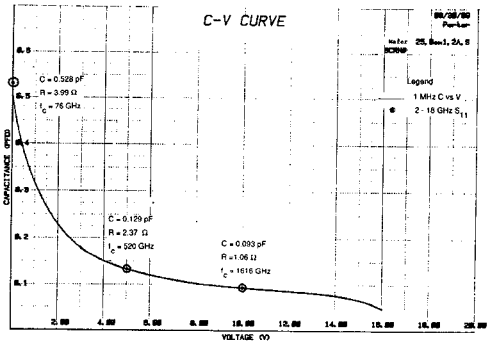

Figure 6. 2-18 GHz Varactor Characterization Data Compared to the 1-MHZ V vs V data

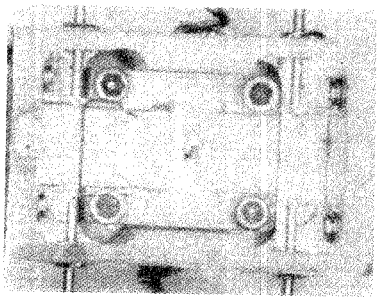

Figure 7. MMIC VCO3 Mounted in the Test Fixture Described in the Text

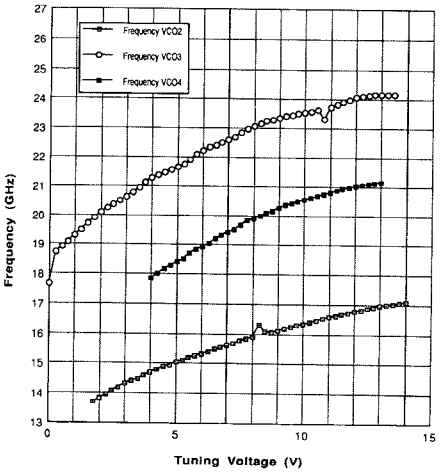

Figure 8. Frequency vs Tuning Voltage for Three Different MMIC VCO Chips

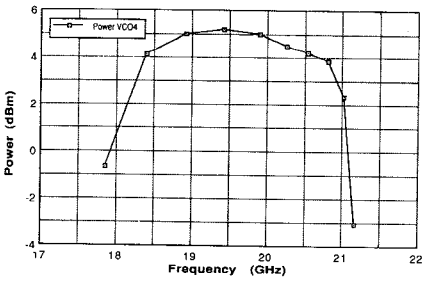

Figure 9. Output Power vs Frequency Curve for the VCO4 Chip